Kneron KL520 series AI SoC

HW design guide

Version 2.1

Revision History:

version	description	date
0.1	Initial version	2019/3/28
2.0	Add reference schematic	2019/8/5
2.1	Add mechanic design guide Add MIPI TX reference schematic	2019/9/18
2.2	Update Figure-5, GND merge	2020/03/26
2.3	Add door lock application	
2.4	Update RREF resistor value Update OM resistor value	2022/06/21

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Figure List

1 Overview

1.1 General description

Kneron KL520 series is an AI SoC targeting smart-home and IoT segment with Kneron NPU core inside to accelerate neural network processing and enabling devices with edge AI ability to achieve Kneron's AI everywhere vision.

This document introduces something that is related to HW design and may need some attention before we start to make KL520 boards.

2 HW reference schematic

There are three power domains in the KNERON KL520 AISC and it includes RTC, Default and NPU power domain. Power domains turned on/off using external power switches controlled by the software through SCU pwerctrl pin. Each domain has its own POR.

There are five power modes for KNERON KL520: RTC mode, Always-on mode, Full Function mode, Retention mode and Deep Retention (Softoff) mode.

The Deep Retention mode is used to shut down the supplies power of all blocks, except the logic in the

RTC domain and DDR memory is in self-refresh state in this mode. The system power consumption is the lowest but it needs longer recovery time for system wake up.

The shows the switchable power when system is entering soft off mode and DDR SRAM keep on the self-refresh state.

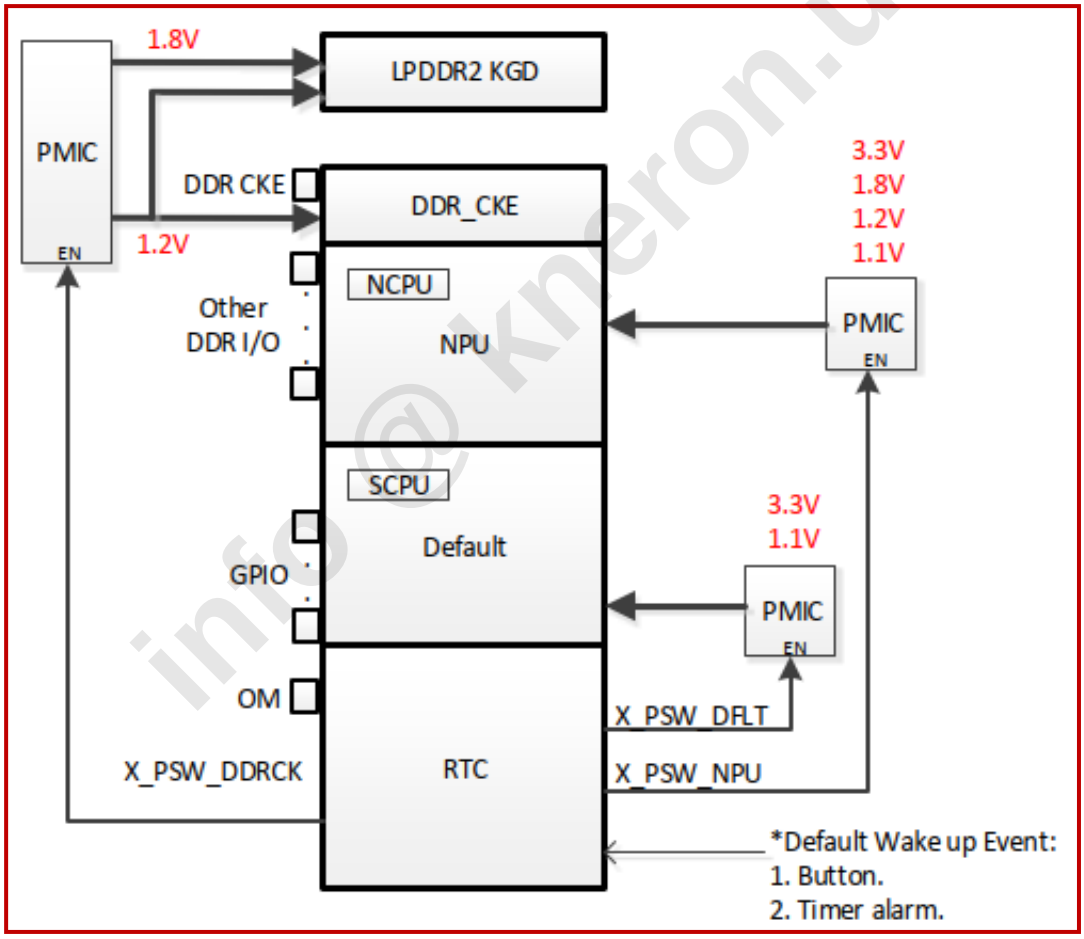

Figure 1 - KNERON KL520 Switchable Power.

2.1 Power

2.1.1Power topology

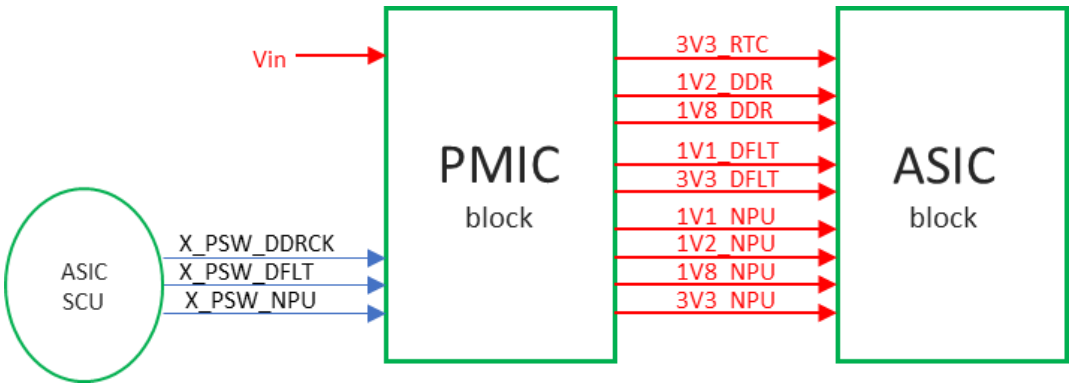

Figure 2 – Power topology

2.1.2PMIC block

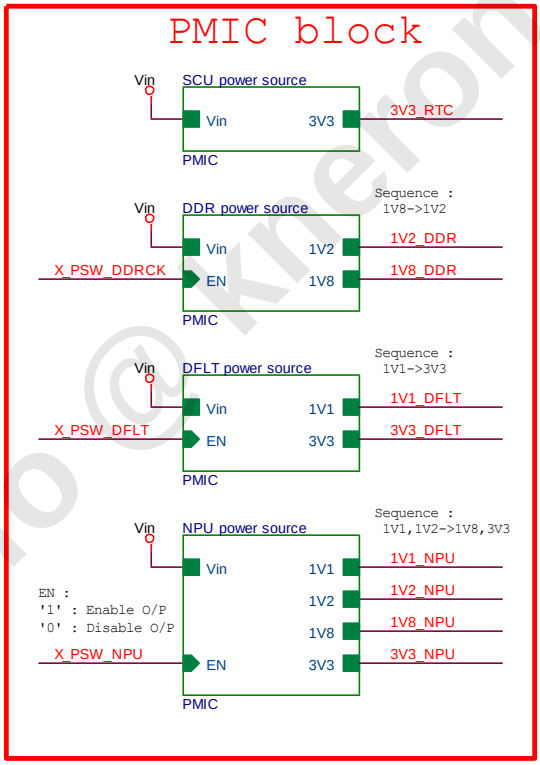

Figure 3 – Power topology: PMIC block

2.1.3ASIC block

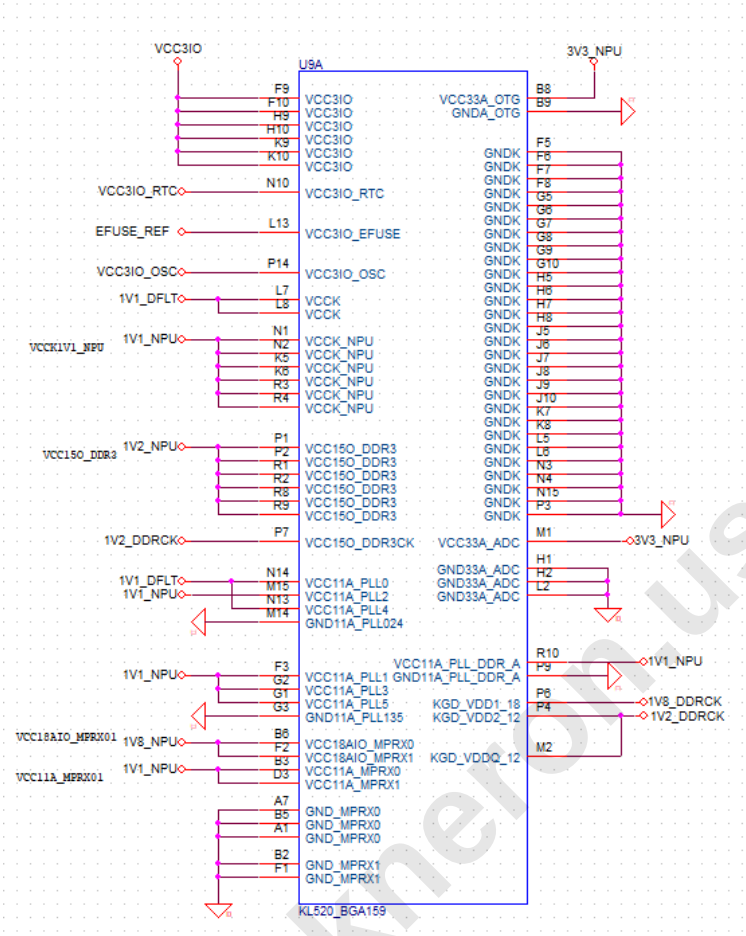

Figure 4 - Power topology: KL520

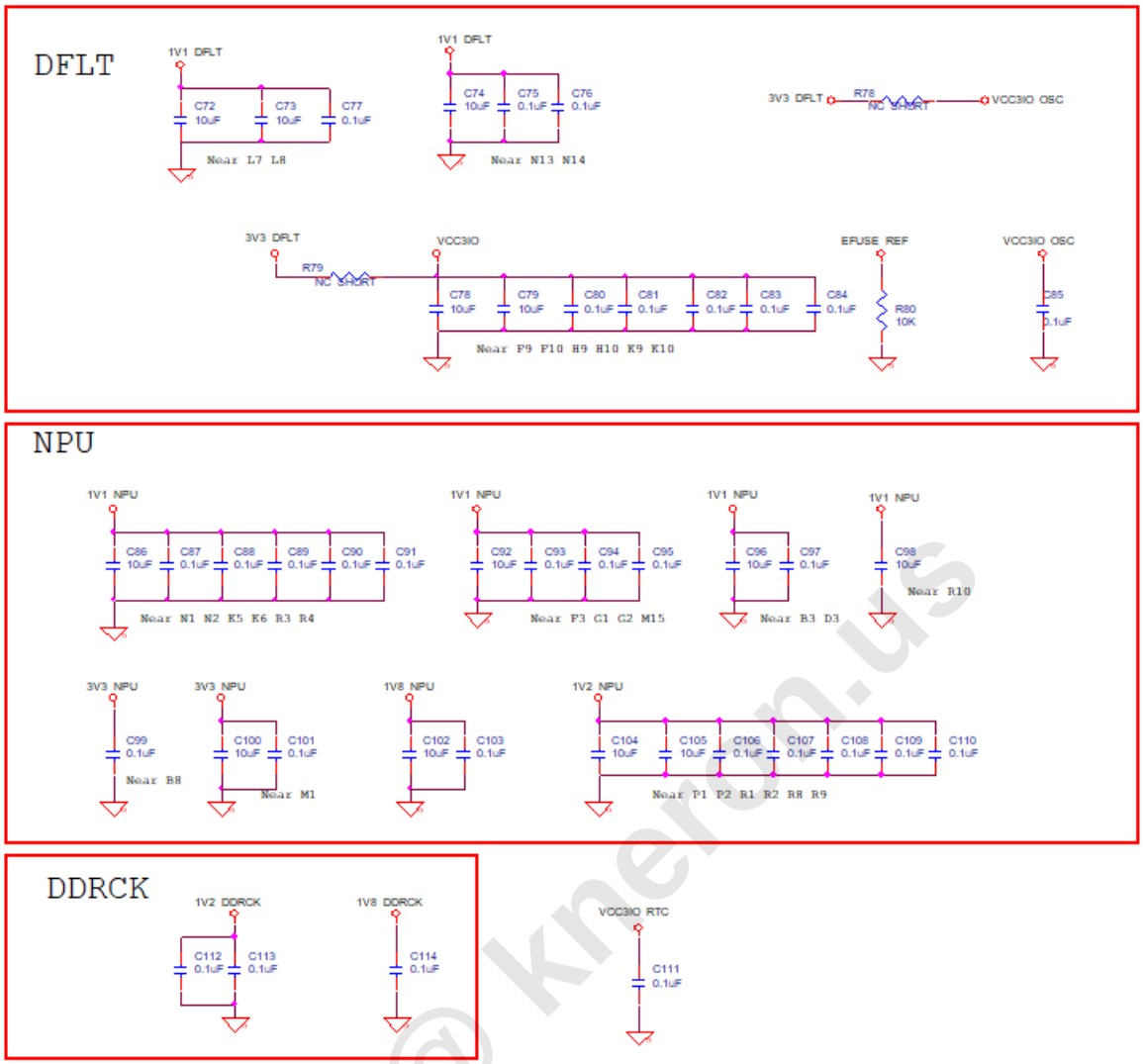

Figure 5 - Power topology: KL520 bypass capacitors

2.2 USB 2.0

There are three different application regarding USB, here's the example for how to do this application from schematic point of view.

2.2.1 USB 2.0: Host Mode

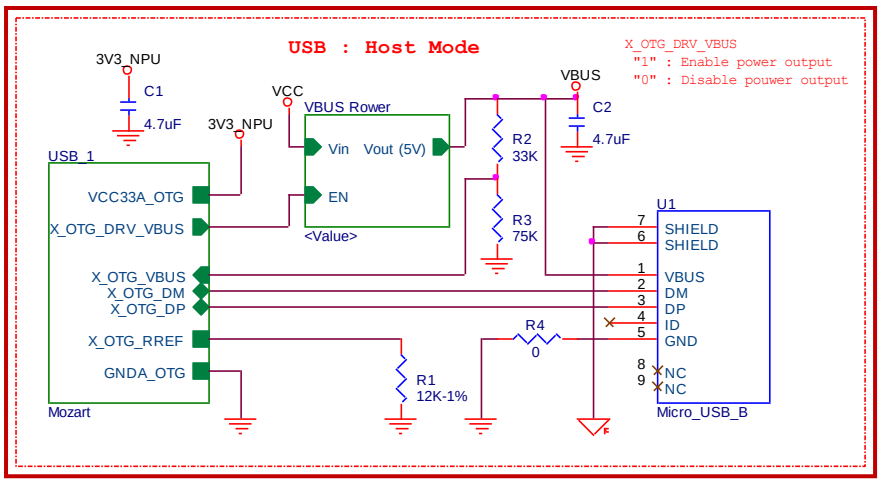

Figure 6 – USB 2.0 schematic reference: Host Mode

2.2.2 USB 2.0: Device Mode

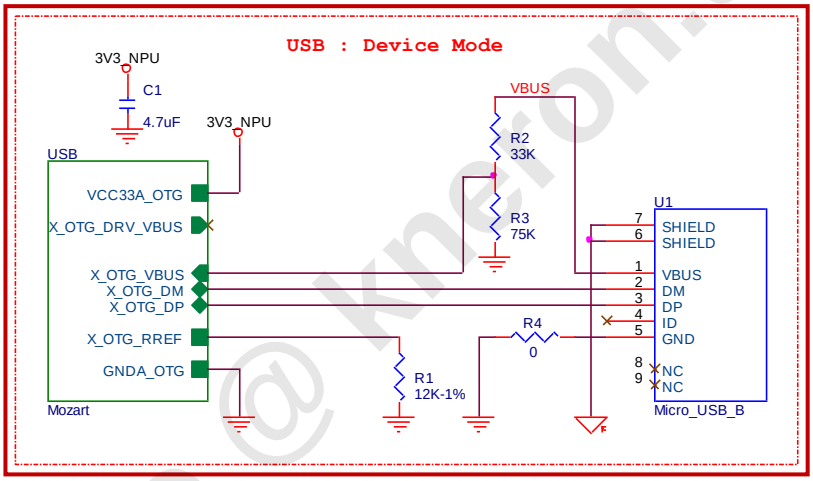

Figure 7 – USB 2.0 schematic reference: Device Mode

2.2.3 USB 2.0: Companion Mode

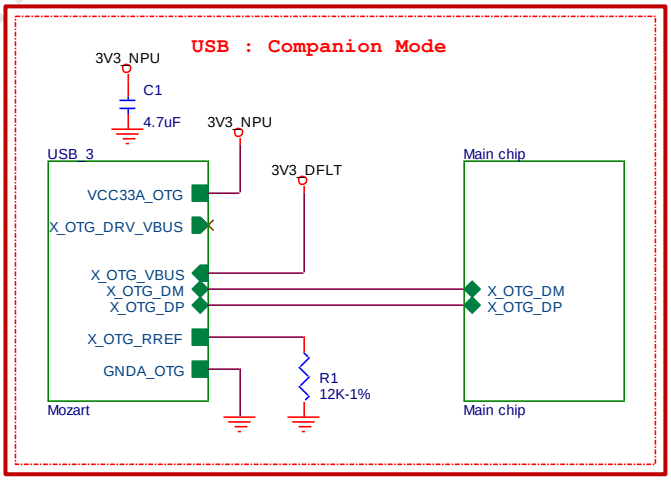

Figure 8 – USB 2.0 schematic reference: Companion Mode

2.2.4 USB 2.0: Not used

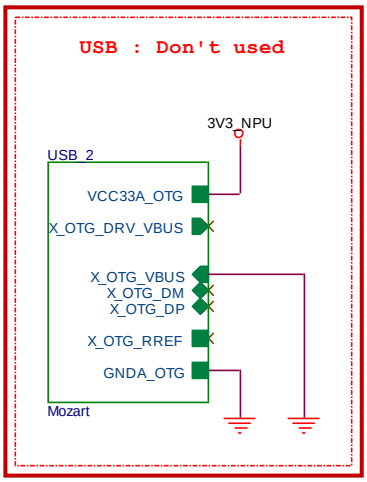

Figure 9 – USB 2.0 schematic reference: Not used

2.3 Bootstrap pin

Bootstrap sets the status when KL520 powered up, we would suggest to set to “EVB design” status when we start to do our development. It can allow user to power up via ROM. Once the development is done, we can change to “product design” setup, it will power up from flash.

2.3.1 EVB design

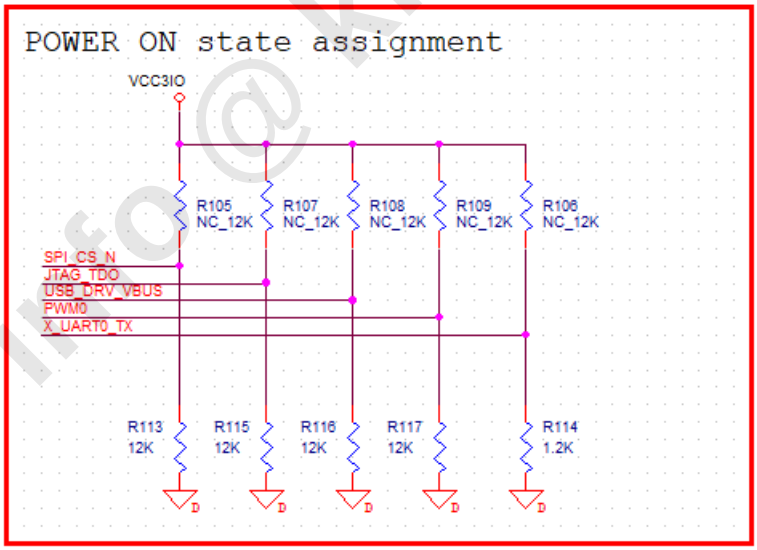

Figure 10 – Bootstrap schematic reference: EVB design

2.3.2 Product design

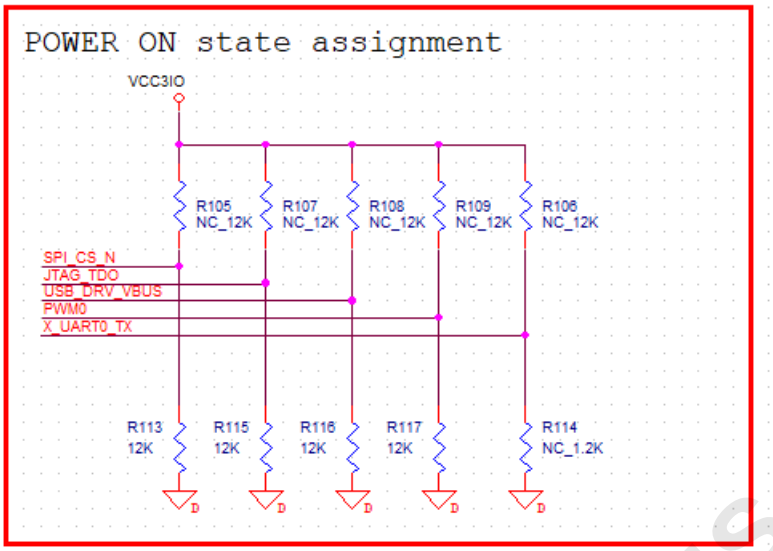

Figure 11 - Bootstrap schematic reference: Product design

2.4 MIPI RX0, RX1

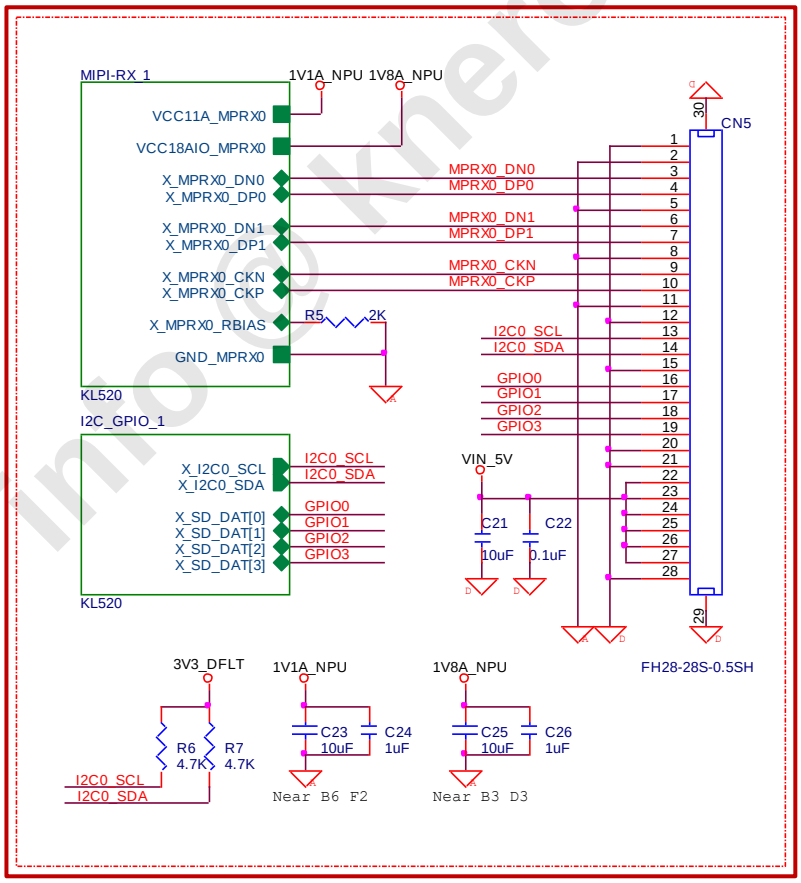

Figure 12 – MIPI RX0, RX1 schematic reference

- Note

If the MIPI Not be used then the X_MPRX0_RBIAS and X_MPRX1_RBIAS can be floated.

2.5 MIPI TX

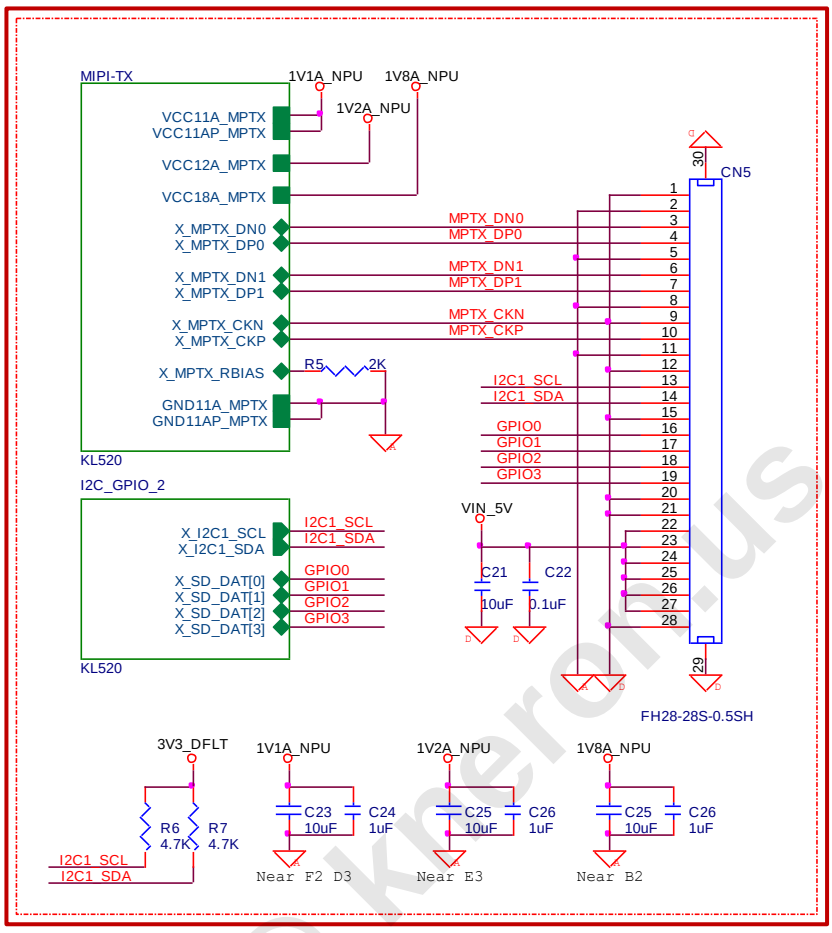

Figure 13 – MIPI TX schematic reference

2.6 XTAL

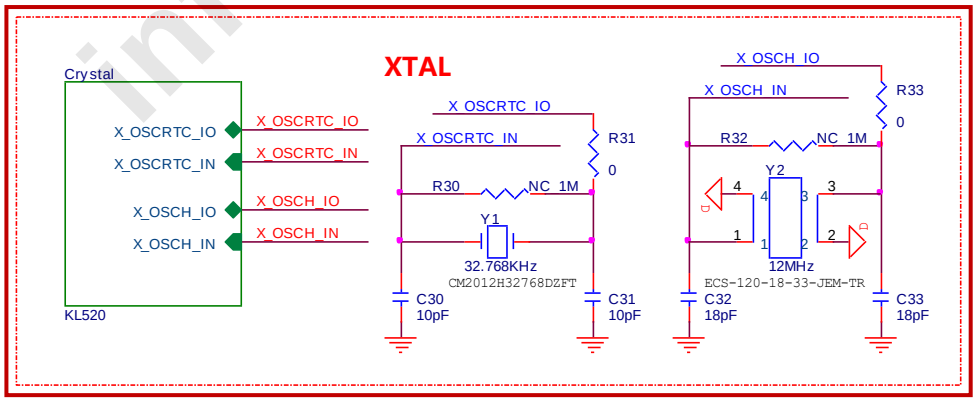

Figure 14– Crystal schematic reference

- Note

These crystals should be placed as close to KL520 as possible.

2.7 ADC

2.7.1 ADC : used

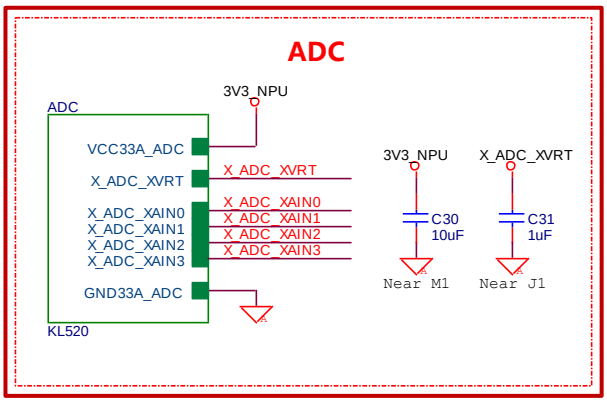

Figure 15– ADC schematic reference

2.7.2 ADC : Not used

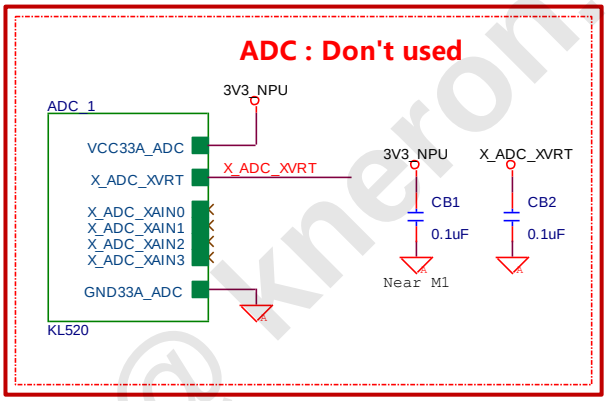

Figure 16 - ADC schematic reference (Not used)

3 HW layout design guide line

3.1 Routing on Power Decoupling cap.

As we mentioned in Chapter2.1, The routing of the capacitor (normally 0603 or 0402 package) should be optimized to achieve lowest inductance. It is recommended to keep the power trace length (from the package pads to the VIAs) as short as possible. Also, we would recommend to avoid sharing the same via with two or more decoupling capacitors.

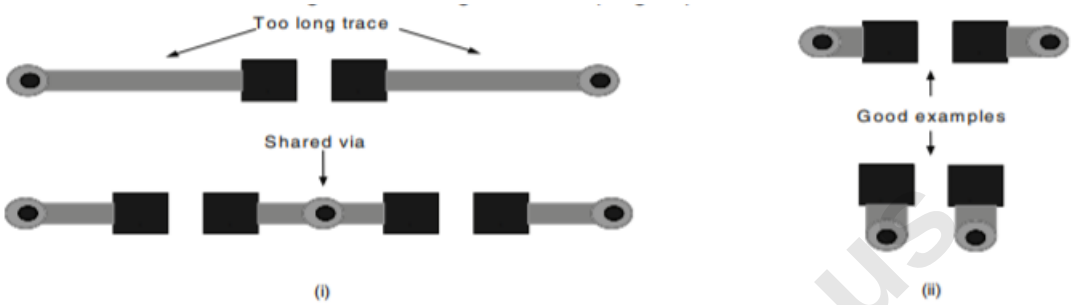

Figure 17- routing example for decoupling capacitors.

Please also follow those rules:

1. Please use plane on GND
2. De-cap placement rule: 1uF, 0.1uF to chip distance < 100mil
3. 1V1_DFLT, 3V3_DFLT, 1V1_NPU, 1V2_NPU must be used the power plane. For other power, the PCB trace width as possible as large than 40 mail
4. Altera also provide the very good examples for de-cap layout as the following figure:

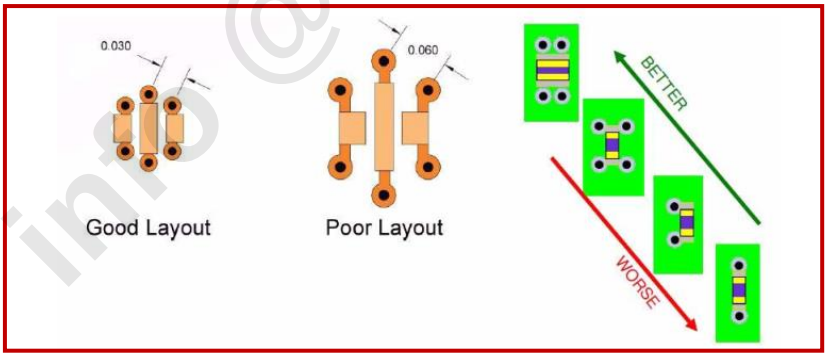

Figure 18- de-cap layout example

3.2 MIPI traces

KL520-series provides a high-resolution high-speed flexible interconnection of the MIPI CSI transceiver. It is compliant with the Camera Serial Interface 2 (CSI-2) and supports MIPI Alliance specifications. The supported data rate is up to 1.2 Gbps per lane and scalable from one to two data lanes.

There are some guide lines for MIPI traces:

- MPRX*CKP/N, MPTX*DP/N and MPRX*DP/N pairs should be routed with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).
- These differential pairs should have the same length. The length difference of these differential pairs should within 5 mils.
- Keep away from other high-speed signals.
- Route all the differential pair on the same layer.
- Each pair should be separated by 3 times of its trace width.
- Leave unused MIPI terminals (MPRX*CKP/N, MPTX*DP/N and MPRX*DP/N) unconnected.
- The number of used VIAs should be as small as possible. Suggested number is less than two.
- There should be a ground plane as reference plane on its adjacent layer.
- Do not route differential pairs over any plane split.

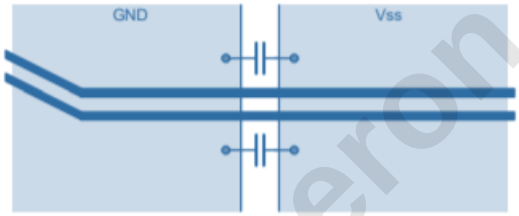

Figure 19- avoid routing across a split plane.

- Adding test points will cause impedance variation. It may impact signal quality. If test points needed, they should be placed in series and symmetrically.
- The maximum trace length over FR4 pcb is around 25~30cm.

3.3 I2C

There's no specific layout requirement for I2C. The I2 C interface (SDA and SCL pins) requires external pull-up resistors to VCCIO for proper operation. If the I2 C interface is not used, then it should be pulled-down or tied directly to GND.

3.4 GPIOs

The GPIO are used for various purposes. Please refer to the KL520 datasheet for functional details of each GPIO. The GPIO do not have any internal pull-up or pull-down resistors. When a GPIO is pulled-up, it should be pulled-up to the VCCIO supply. Unused GPIOs should be pulled-down or tied to GND.

3.5 TEST Pins

MPRX1_RBIAS, MPRX0_RBIAS, OTG_RREF, RBias, KGD_ZQ, DDRUP and DDRDN pins are reserved pins and

are intended for Kneron use only.

- MPRX1_RBIAS and MPRX0_RBIAS are connect 2Kohm resistor to GND.
- OTG_RREF is connect 12Kohm to GND
- OM is connected to Ground through a 1KΩ resistor
- DDRUP is connect 240ohm to GND
- DDRDN is connect 240ohm to VCC150O_DDR3
- KGD_ZQ is connect 240ohm to GND

Users can simply refer to KL520 reference schematic for how to make these connections in detail.

3.6 Clock traces

As we mentioned in Chapter2.2, there are two clock sources in KL520, 32.768KHz and 12MHz.

A series resistor is recommended near each clock source to reduce EMI. If possible, bury these clock trace in the inner layer or minimize the distance between KL520 and these two crystals.

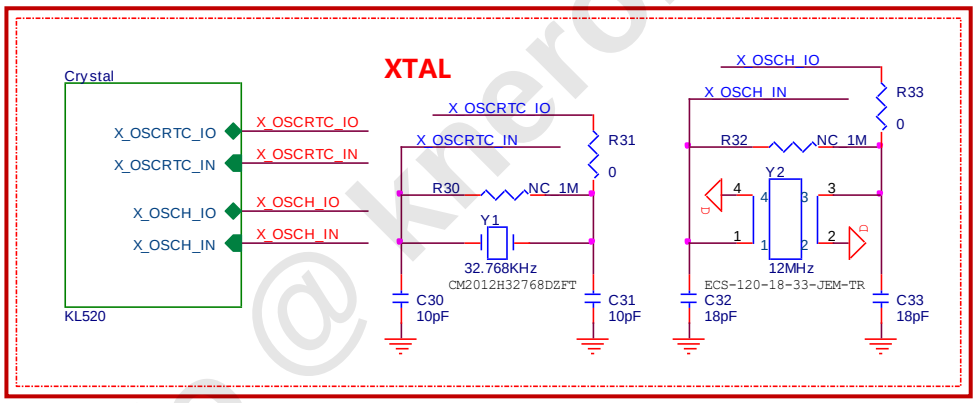

Figure 20- reserve a series resistor to avoid EMI problem.

3.7 USB traces

USB in KL520-series can be configured as host, device, and OTG applications, which enable an easy connection between the USB peripherals and any USB-ready product.

Bellowing are the recommended routing rules for USB traces.

- Route OTG_DM and OTG_DP as 90ohm differential pair
- There should be a reference ground plane adjacent to routing layer
- Route OTG_DM and OTG_DP as short as possible.
- Keep away from other high-speed signals.
- Do not route OTG_DM and OTG_DP pair over any plane split.

- Keep away from edge of reference plane
- Always provide a good return path (ground) for current
- Adding test points will cause impedance variation. It may impact signal quality. If test points needed, they should be placed in series and symmetrically.

Figure 21- recommended routing of test points on differential pair

3.8 SPI traces

KL520-series contains SPI interface controller to execute the SPI Flash command as ROM and link with other devices.

3.8.1Clock Signal routing

When routing the clock signal, special cares should be taken.

There are some major notes for the clock routing.

- The clock trace should be separated from other signal from 3 time of its trace width.

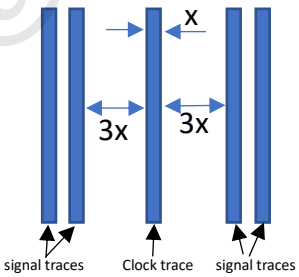

Figure 22- Separate clock from other signals.

- Use as less VIAs as possible.
- There should be a reference plane adjacent to clock routing plane and the reference plane should be continuous.
- Route clock trace as straight as possible. To avoid serpentine trace for clock.

3.8.2 Data signal routing

There are some notes for data signals:

- Data bus should be routed with matching length to the reference of clock. We

recommended within +/-150 mils.

- Signal traces should have a solid reference plane (power or ground).

3.9 SDIO traces

KL520 offers SDIO interface that enables us to use SDIO BT/Wifi module.

These are the notes for the SDIO traces guide line:

- Do not leave any stubs on traces and limit the length of DATA trace to not exceed that of the CLK trace
- Match the lengths of the SDIO lines to within ±100 mils. Note that the time delay is about 16.7 ps for every 100 mils of length
- Separate the SDIO_CLK line from the SDIO CMD and DATA lines (we would suggest minimum distance between SDIO_CLK and SDIO CMD/ SDIO DATA is two time of its trace width). Routing the SDIO_CLK line parallel and close to command and data lines can cause glitches on the bus, thus affecting SDIO operation

3.10 UART/PWM/I2S

KL520 implements the most common communication protocol, UART. For black light or LED control, it also offers PWM. Since I2S is a populate audio format provided by many audio devices, KL520-series provides this interface to transfer digital audio data.

These signals do not have specific requirement for hardware point of view. But please keep them away from noisy signals.

4 Design Consideration of smart door lock application

With the KL520, we can turn a door lock into a door opener that has face recognition function.

Figure 23-Using KL520 as a smart door lock

For the smart door application, designers need to pay attention about KL520 power arrangement. The door lock is powered by battery and user is not always use door lock all the time. It needs to have low power consumption at sleep mode (or called RTC mode.) at uA order.

4.1 Power arrangement in door lock application

Bellow figure shows the power arrangement in door lock application. From bellowing figure, we can find that we have an additional switch on it. The reason for the switch is that we can switch the 5V power off to avoid the leakage current on the PMIC in RTC mode.

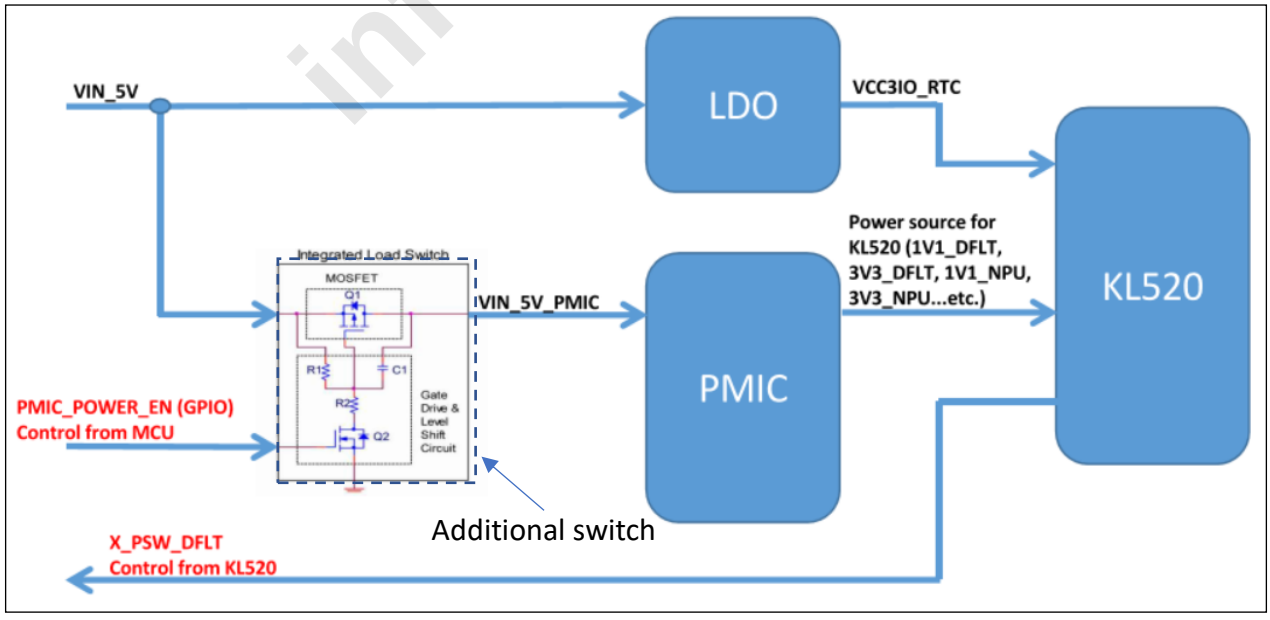

Figure 24- power arrangement in door lock application

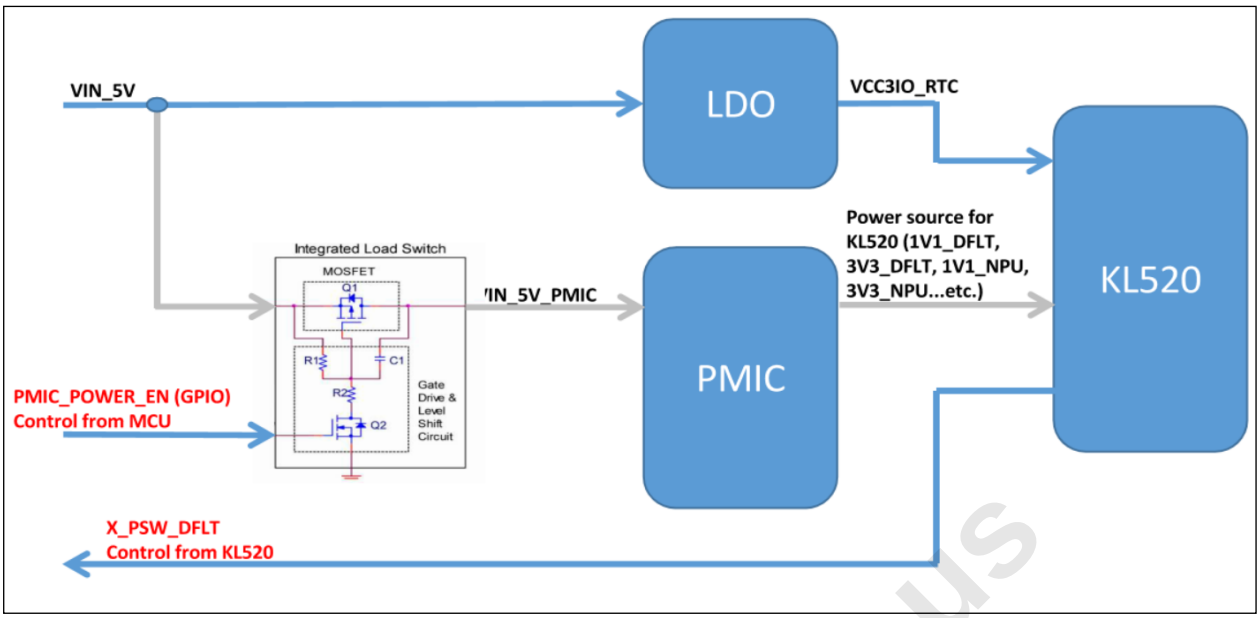

Figure 25- power off the 5V input in RTC mode to save more current

4.2 Control interface between KL520 and host

There are several IOs that may need to connect to KL520:

- USB
- UARTn_TX/RX (except UART0)
- X_RESET_N
- X_PTN
- X_PSW_DFLT
- PMIC_POWER_EN (GPIO)
- JTAG

4.3 Block Diagram

Bellowing is the block diagram that shows how these IOs are connect to KL520:

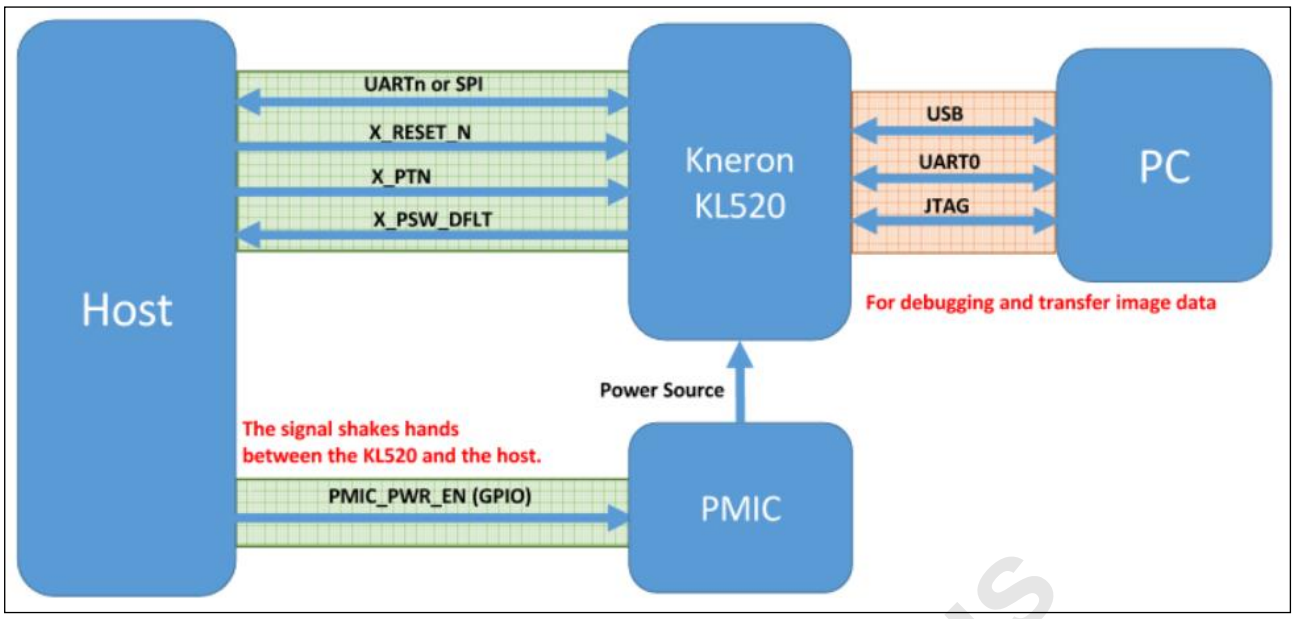

Figure 26 – block diagram of the IOs that connect to KL520

4.4 IO description

4.4.1 USB interface

This interface is reserved for debugging. For example, capturing the images from DDR and FW update.

4.4.2 UARTn and SPI (except UART0)

Where n= 1~4. UART0 is the default interface used for KL520 debugging. For example, the debugging message.

UARTn/SPI is the interface between AP and KL520. For example, returning the recognition result to AP.

4.4.3 X_RESET_N

X_RESET_N is connected to the host. The host can control this pin to reset the KL520.

4.4.4 X_PTN

X_PTN is connected to host. Host can control this pin to turn on or turn off the KL520.

4.4.5 X_PSW_DFLT

X_PSW_DFLT should be connected to the host. X_PSW_DFLT will change the voltage from high to low when KL520 entered RTC mode.

4.4.6 PMIC_POWER_EN (GPIO)

As we mentioned in 4.1, X_PSW_DFLT will notify the host before the KL520 turns off the internal power and enters RTC mode. HOST_POWER_ON from the host will turn off PMIC.

4.4.7 JTAG

JTAG interface is for KL520 debugging.

4.5 Timing recommendation of entering/existing RTC mode.

This chapter will show the flow of how to enter and exist RTC mode.

4.5.1 The flow of entering RTC mode.

The host flow of entering RTC mode will be like:

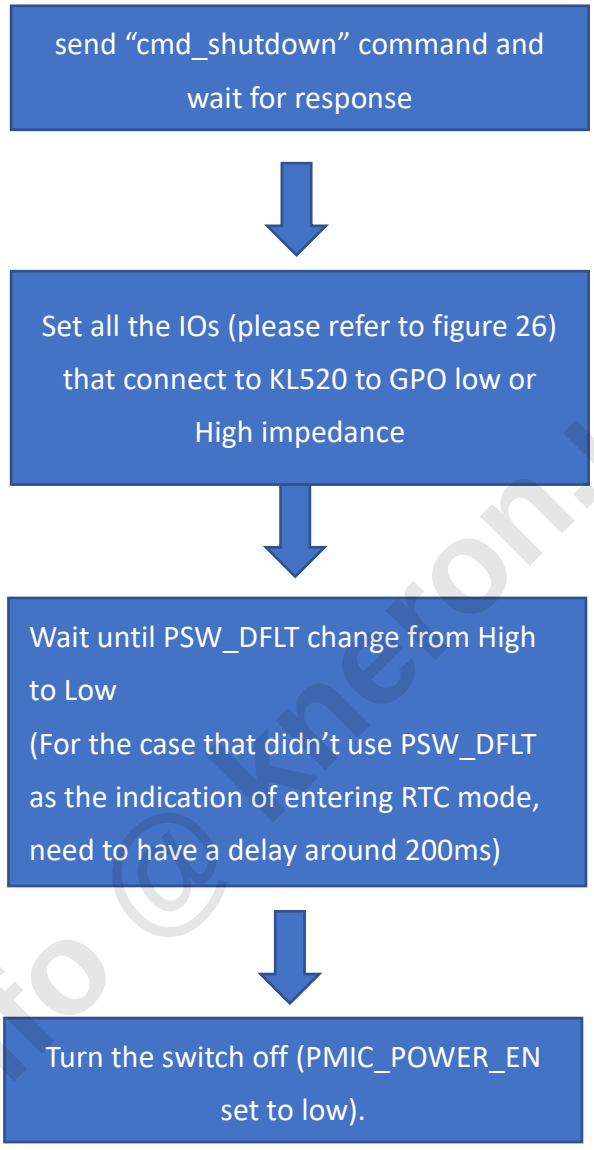

Figure 27 – the flow of entering RTC mode

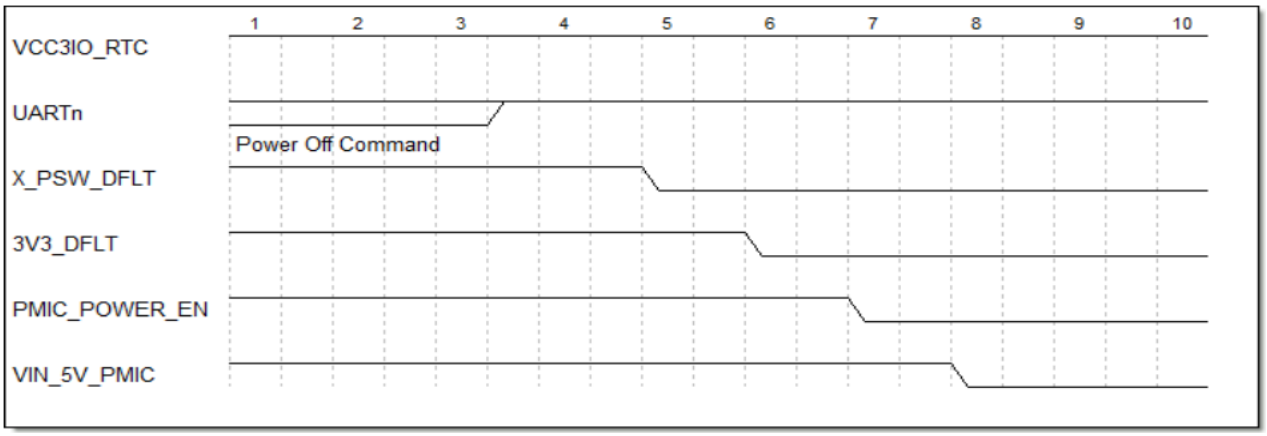

Figure 28 – timing diagram example of entering RTC mode

4.5.2 The flow of existing RTC mode

The host flow of existing RTC mode would be like:

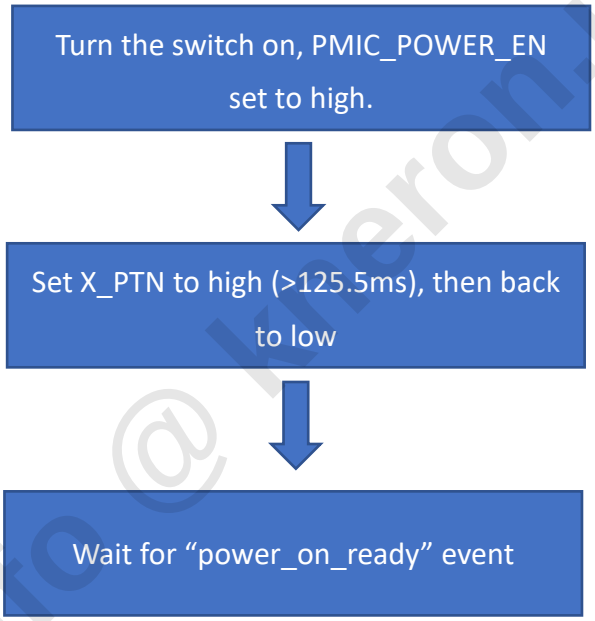

Figure 29 – the flow of existing RTC mode

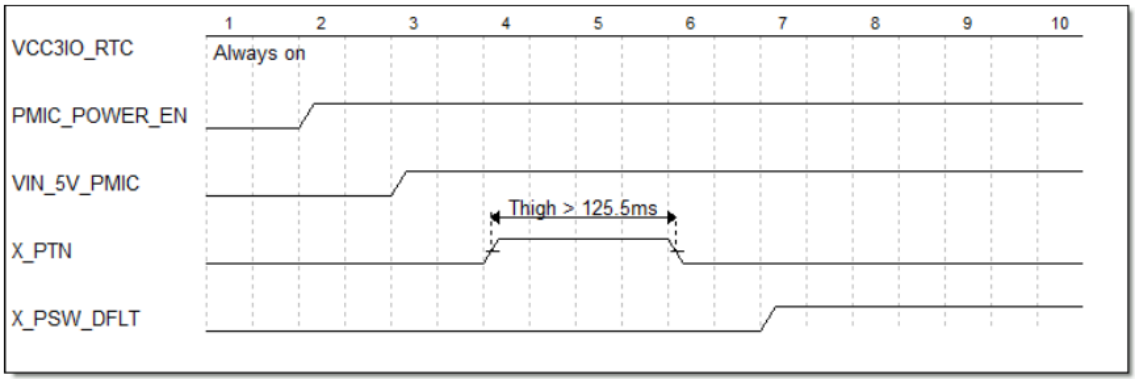

Figure 30 – timing diagram of existing RTC mode

4.6 Mechanic considerations

Besides schematic and layout, there are something that may also need to pay some attention. This chapter shows something belong to mechanic design.

4.6.1 Put two cameras at the same base line.

If users want to use two cameras to do such as 3D recognition, please note that we need to put these two cameras at the horizontal line. Please refer to bellow drawing:

Figure 31- Good example of camera placement

Figure 32- Bad example of camera placement.

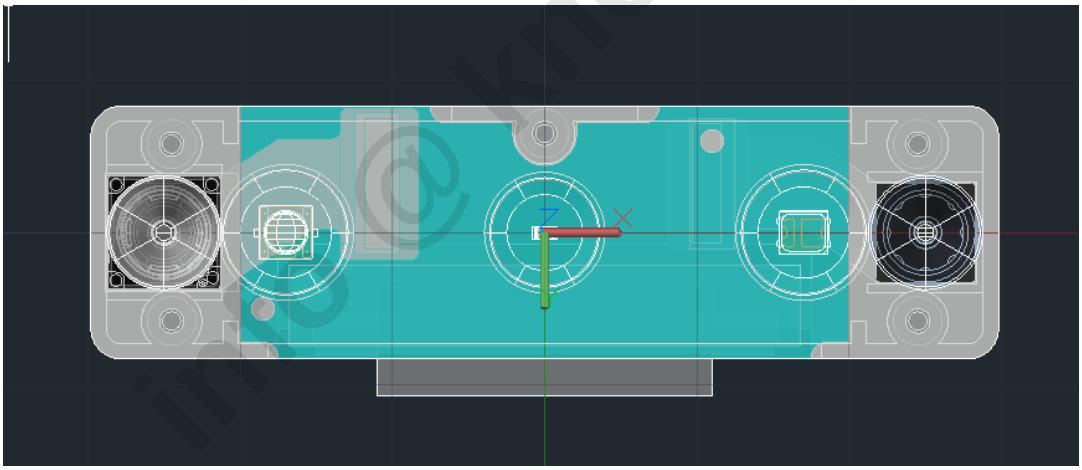

Figure 33- a practical example of two cameras in a mechanic housing.

4.6.2 Minimum distance between two cameras

The suggested minimum distance between two cameras is 5cm.

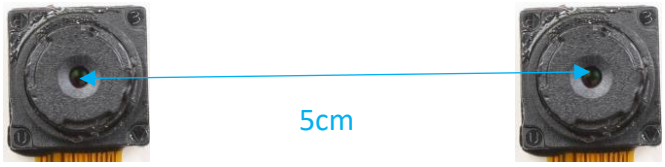

Figure 34- suggested minimum distance between two cameras

4.6.3 Scanning orders

In order to get a good recognition results, we should follow scanning orders like picture show bellow:

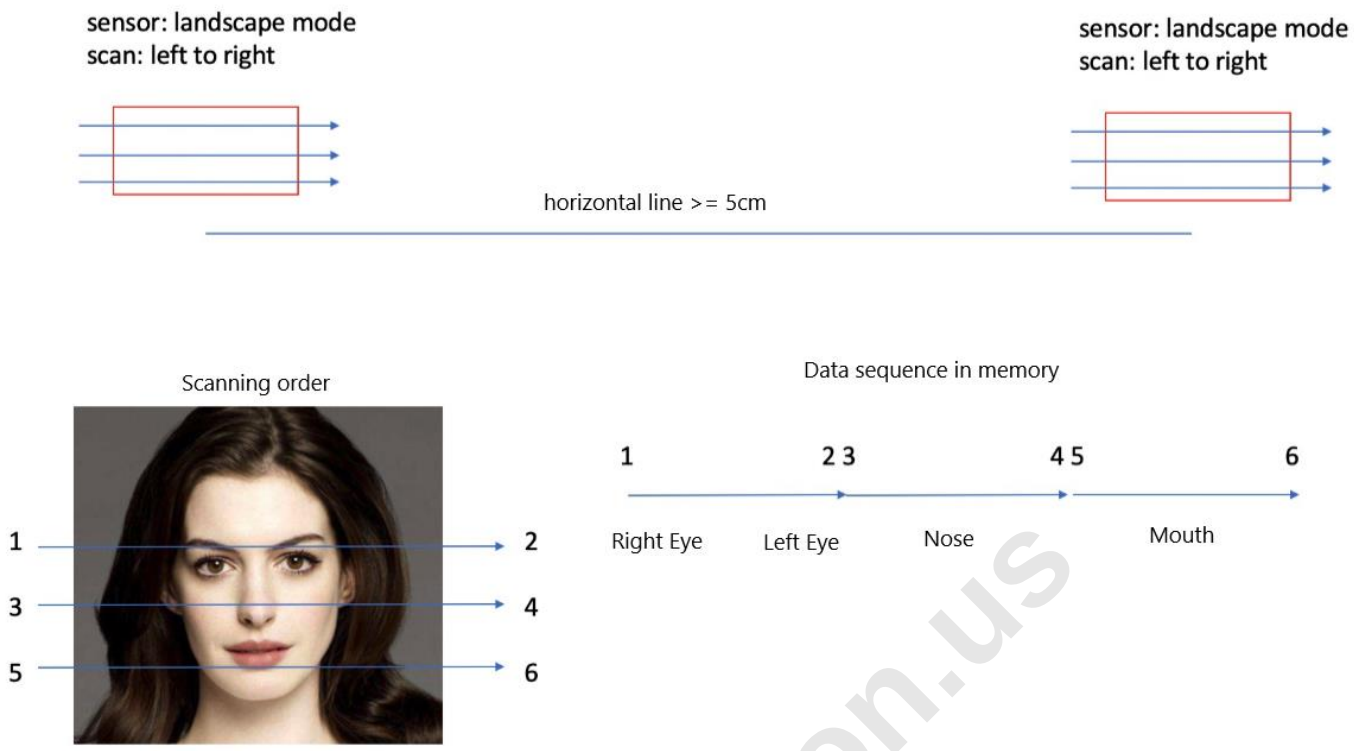

Figure 35- suggested scanning order

4.6.4 How to check camera's scanning order

When we open a camera sensor's datasheet, we may find a picture shows its first pixel and its pixel size:

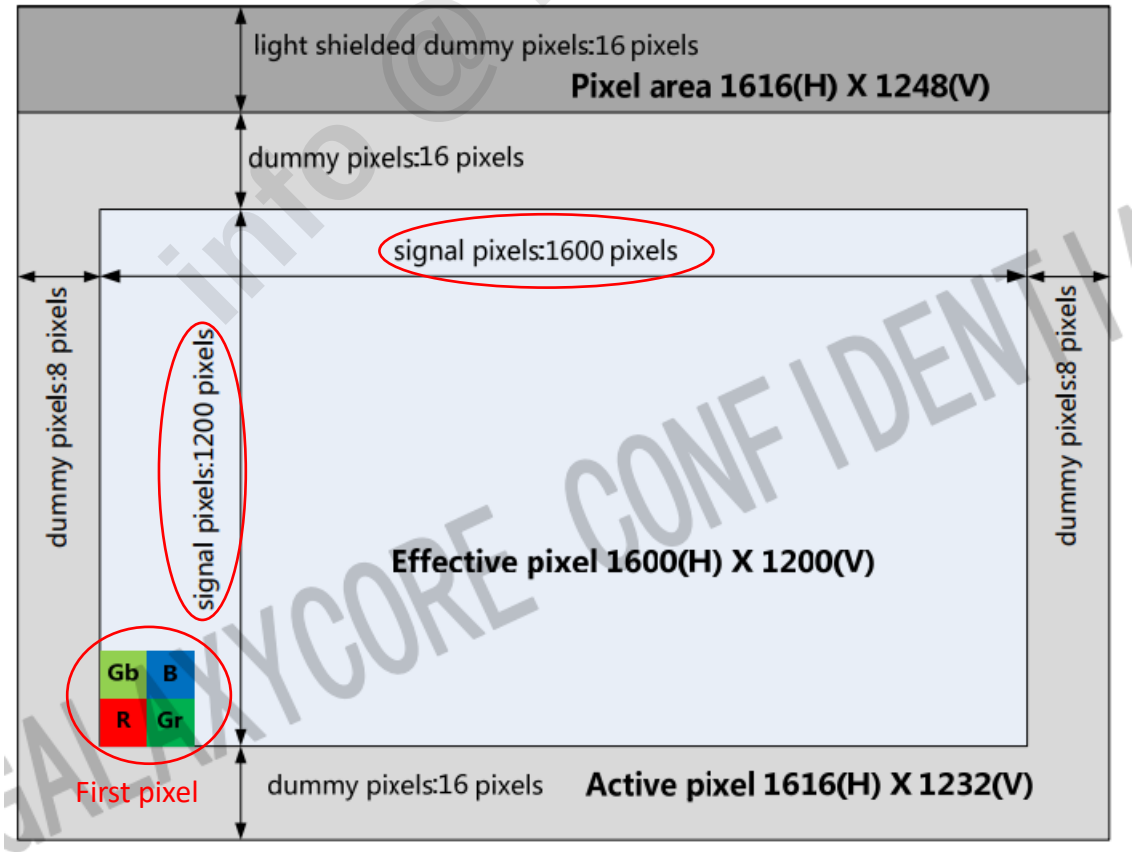

Figure 36- First pixel and camera pixel size.

Normally, the scanning order is horizontal line, like picture bellow:

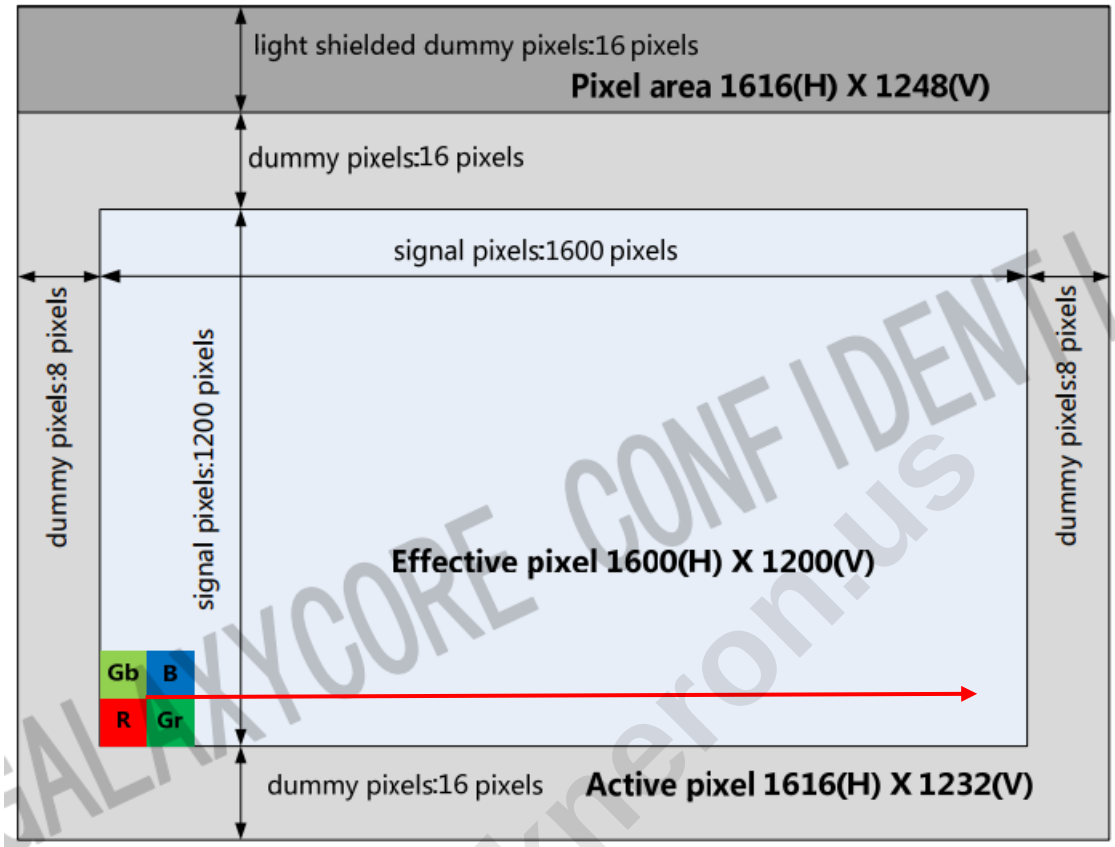

Figure 37- scanning order

The scanning order is along with “1600-pixel side”. Then we can open the datasheet of camera module, we know that scanning order is along with “1600-pixel side”, the scanning order would like picture show bellow:

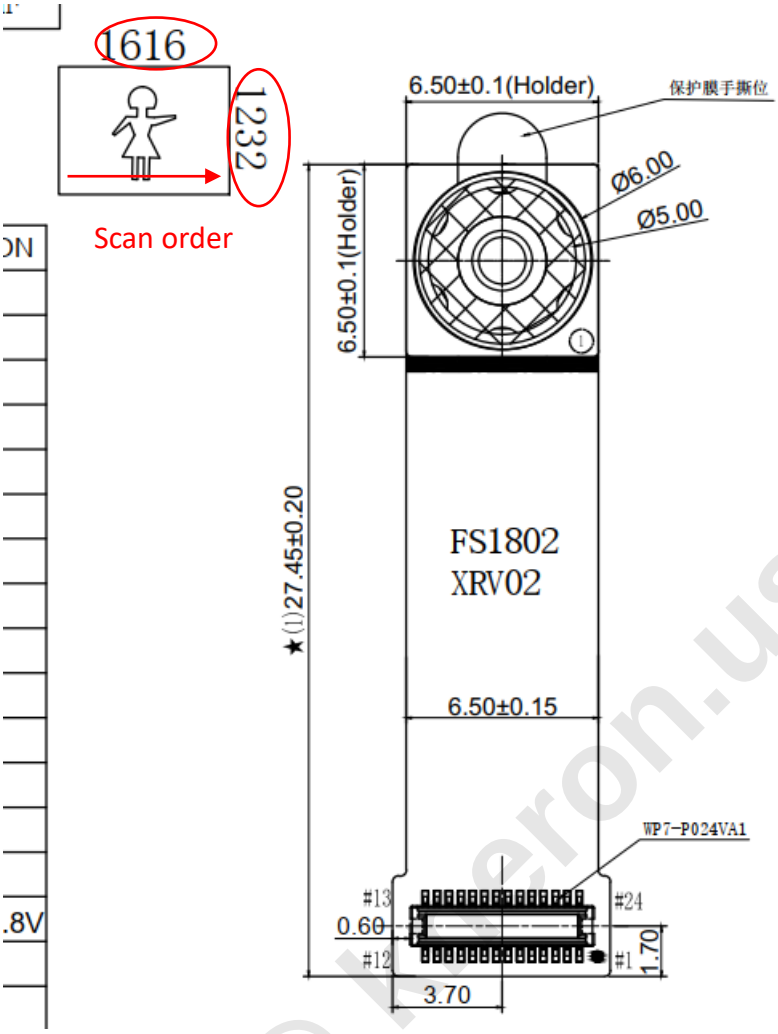

Figure 38- scanning order in camera module

Users may want to ask how we know exactly scanning is start and from which corner:

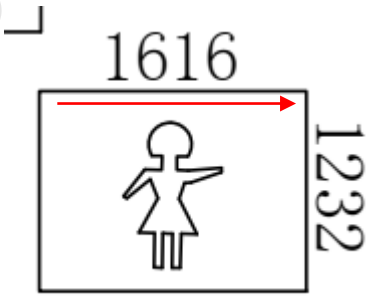

Figure 39- From upper left corner

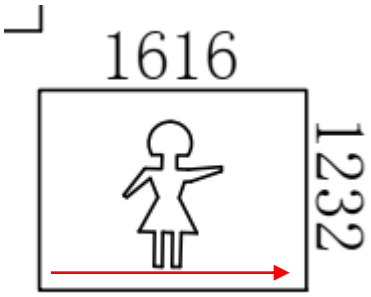

Figure 40- from lower left corner

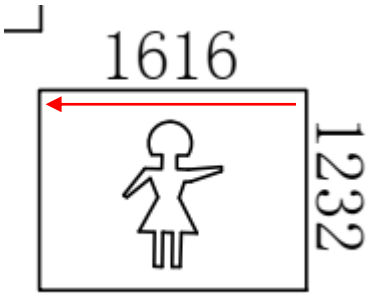

Figure 41- from upper right corner

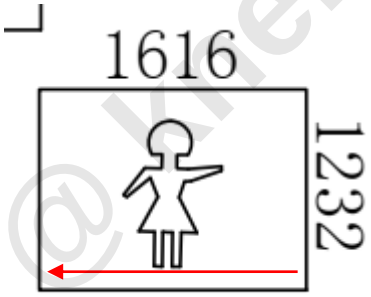

Figure 42- from lower right corner

It’s not really matters, we just need to know which side scanning order is along with. The reason is that normally camera sensor has flip/mirror function, we can use it to adjust to correct the orders we want:

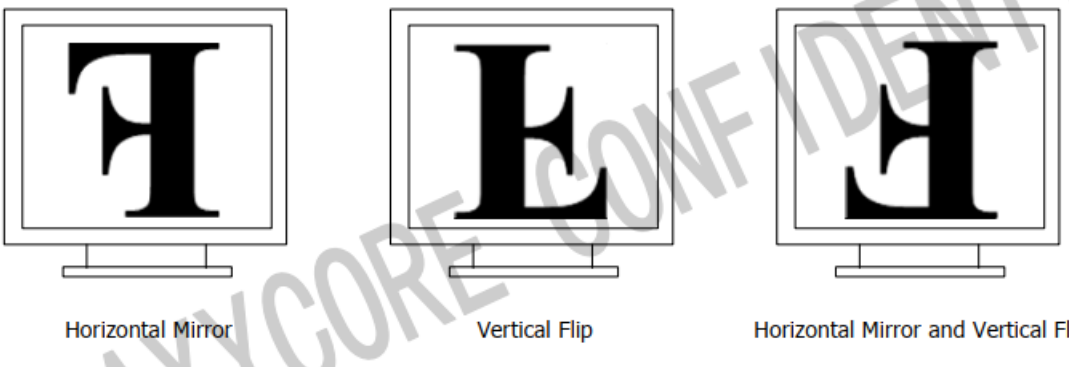

Figure 43- mirror and flip function of camera module.

4.6.5 The opening window of LED

The opening window of LED need to be considered carefully. If this window too small, we will see a noisy, blurry and ringing artifacts after adding smart lock housing.

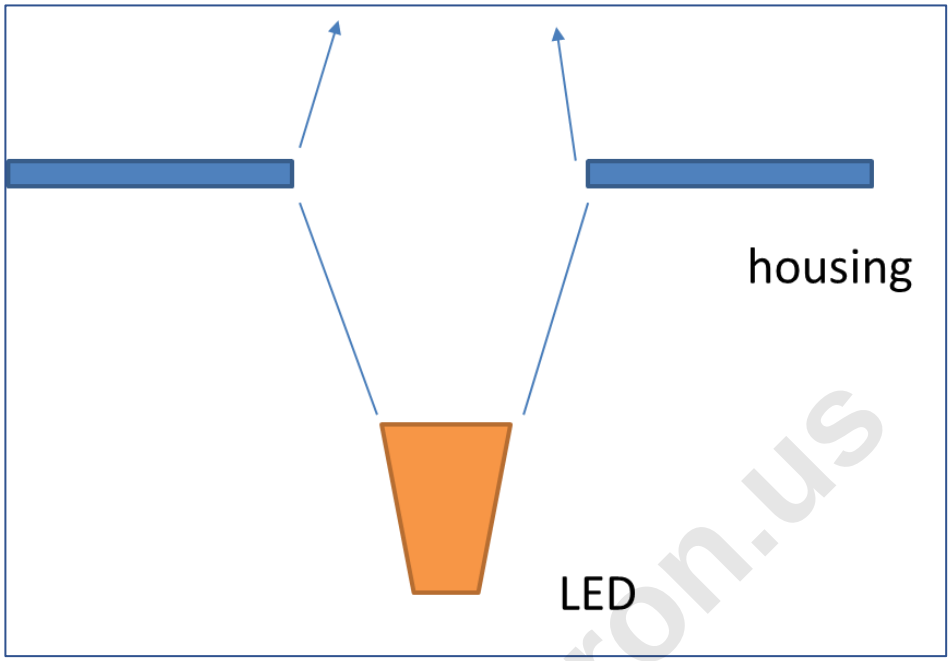

Figure 44 – small opening would cause refraction of light

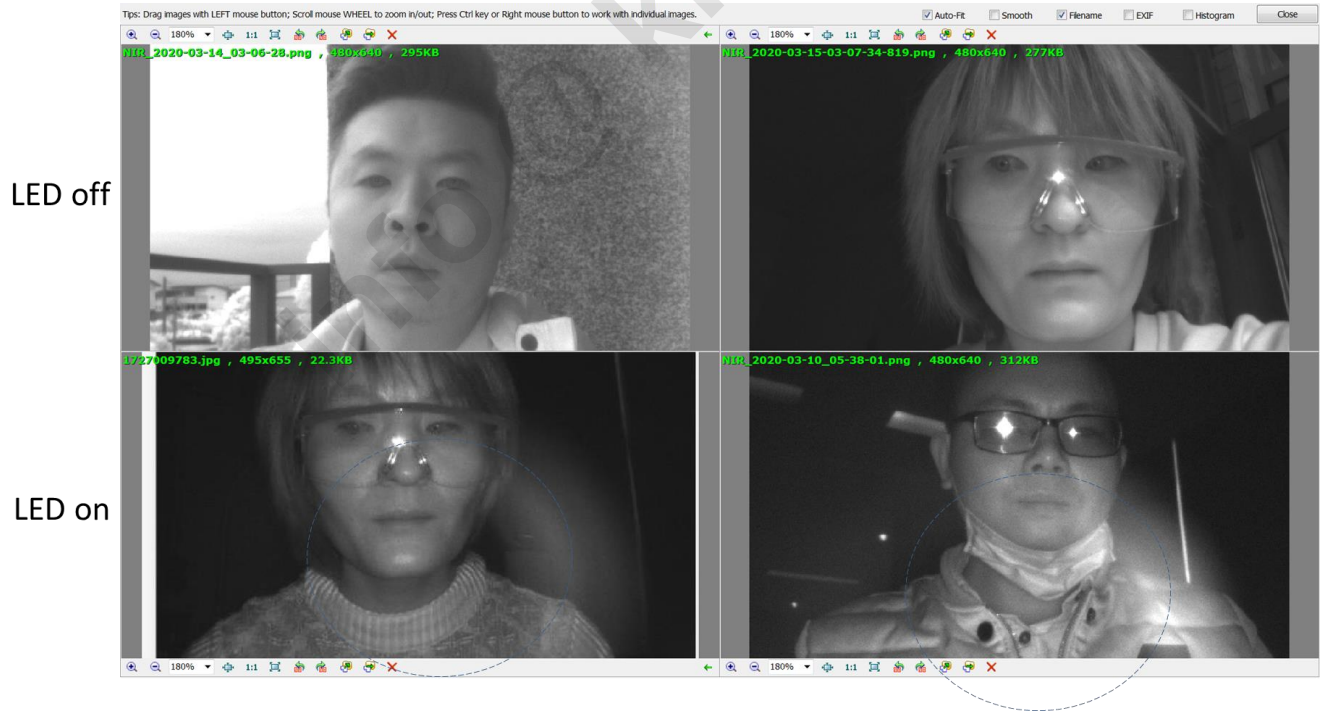

Figure 45 – NIR images, we can see a ring if we turn on the LED

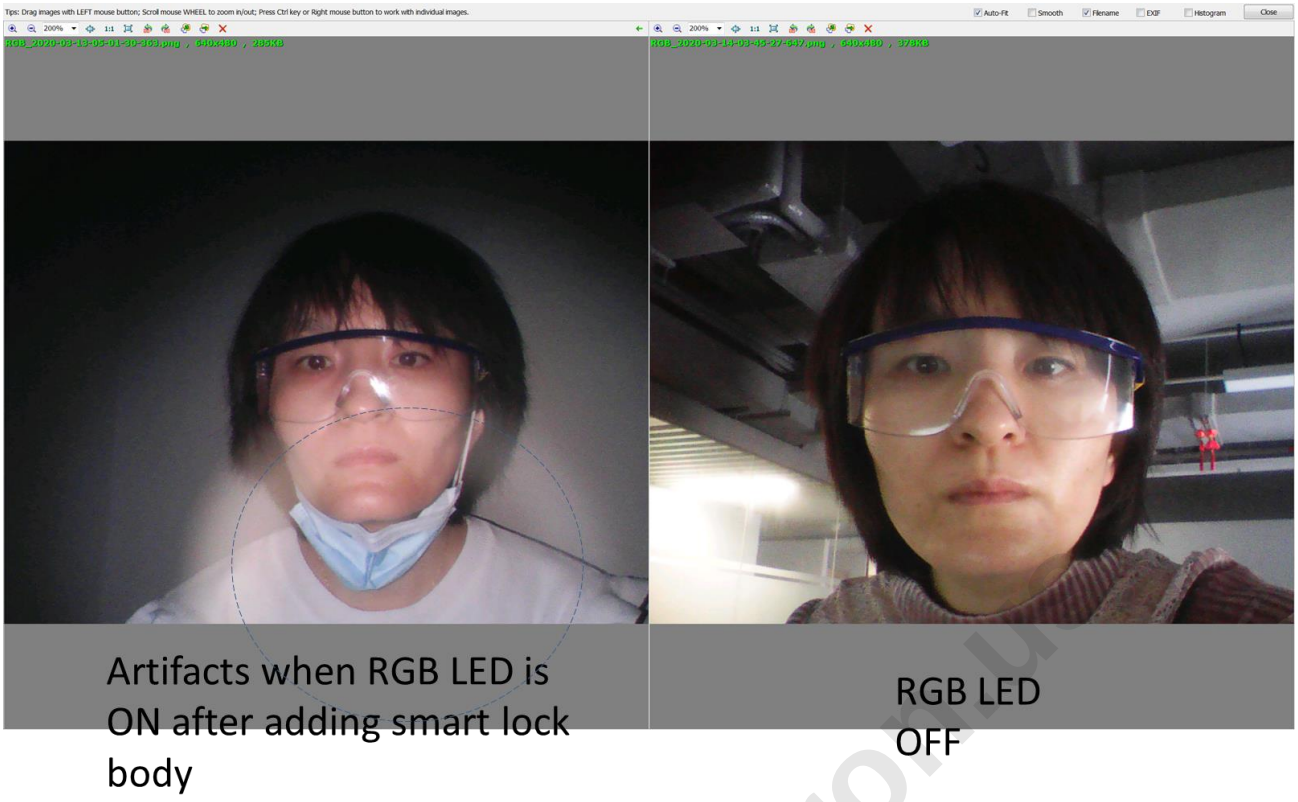

Figure 46 – RGB images, we can see a ring if we turn on the LED

4.6.6 The opening window of cameras

Similar to what we describe in previous chapter, the opening window of LEDs. A bad camera opening design will cause a bad image we got from camera. Some area will be blocked.

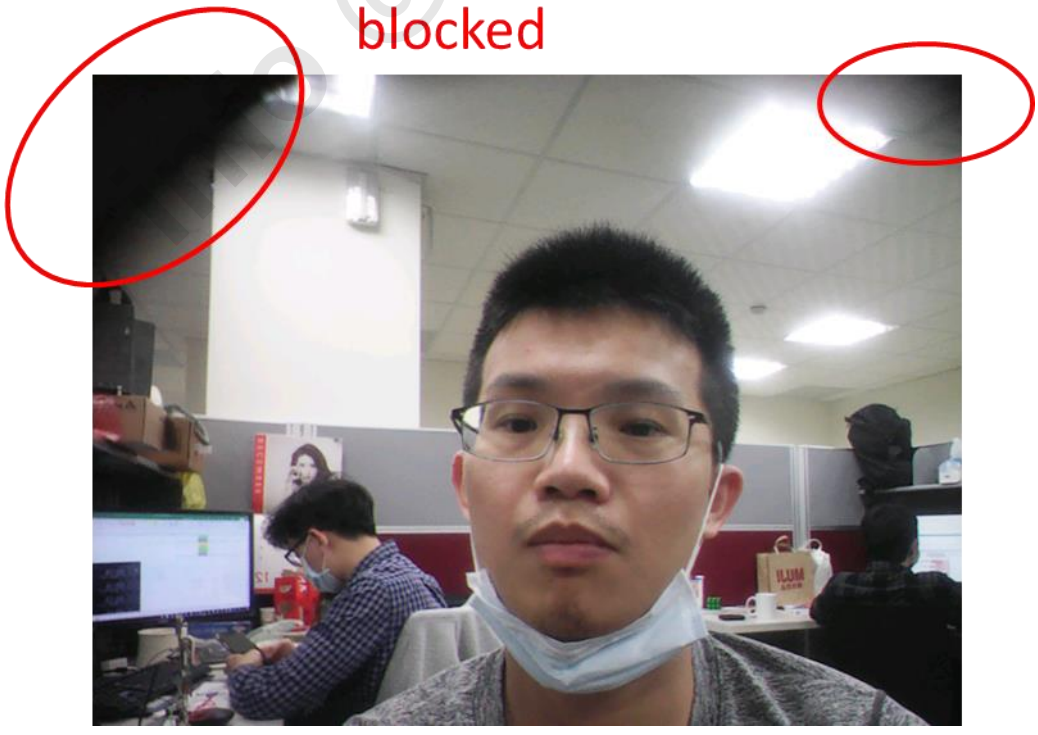

Figure 47 – image corners are blocked.

It is important to double check images from camera when engineers finish the mechanic parts assembly.

4.6.7 Tilt NIR around 6~8 degree (optional)

If possible, we would suggest to tilt NIR camera a bit in order to get more precise 3D result.

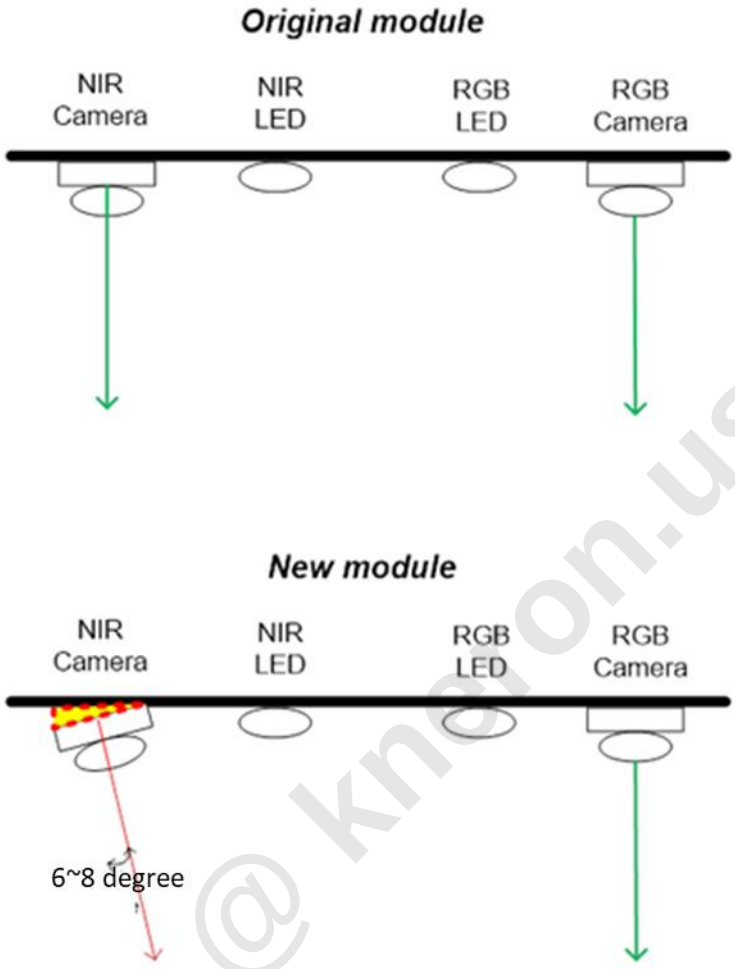

Figure 48 – tilt NIR camera to 6~8 degree