### 1.1.1 CSI Error Report Register (CSIERR, Address = 0x30 ~ 0x31)

**CSI Error Report Register 0 (CSIERR0, Address = 0x30)**

| Bit | Name | Type | Default Value | Description |
|---|---|---|---|---|
| 7 | CD | RO | 0 | Contention Detected<br>When this bit is set, it indicates that either of the data lane signals “ErrContentionLP0” or ”ErrContentionLP1” has asserted. |
| 6 | FCE | RO | 0 | False Control Error<br>When this bit is set, it indicates that either of ErrControl[***n***] has asserted. |
| 5 | HSRT | RO | 0 | High-Speed Receiver Timeout<br>When this bit is set, it indicates that “HS RX Timeout” (HRX-TO) has occurred. |
| 4 | PCR | RO | 0 | PPI Checking Result<br>This bit reflects the value of the output signal, csi_chk_pass_r. |
| 3 | EMECE | RO | 0 | Escape Mode Entry Command Error<br>When this bit is set, it indicates that either of ErrEsc[***n***] has asserted. |
| 2 | ESE | RO | 0 | EoT Sync Error<br>When this bit is set, it indicates that either of ErrEotSyncHS[***n***] has asserted. |
| 1 | SSE | RO | 0 | SoT Sync Error<br>When this bit is set, it indicates that either of ErrSotSyncHS[***n***] has asserted. |
| 0 | SE | RO | 0 | SoT Error<br>When this bit is set, it indicates that either of ErrSotHS[***n***] has asserted. |

**CSI Error Report Register 1 (CSIERR1, Address = 0x31)**

| Bit | Name | Type | Default Value | Description |
|---|---|---|---|---|
| [7:6] | - | RO | 0 | Reserved |
| 5 | ITL | RO | 0 | Invalid Transmission Length |
| 4 | CSIVIDI | RO | 0 | CSI VC ID Invalid |
| 3 | UPT | RO | 0 | Unsupported Packet Type |
| 2 | CE | RO | 0 | Checksum Error (Long packet only) |
| 1 | ECCEM | RO | 0 | ECC Error, multi-bit (Detected but not corrected) |

| Bit | Name | Type | Default Value | Description |
|---|---|---|---|---|
| 0 | ECCES | RO | 0 | ECC Error, single-bit (Detected and corrected) |

### 1.1.2 Interrupt Status Register (INTSTS, Address = 0x33)

**Interrupt Status Register (INTSTS, Address = 0x33)**

| Bit | Name | Type | Default Value | Description |
|---|---|---|---|---|
| 7 | - | RO | 0 | Reserved |
| 6 | RT | RW1C | 0 | Receive Trigger<br>This bit is set when CSIRX receives the trigger events from the PPI signal, RxTriggerEsc. The bus value of RxTriggerEsc can be found in the register ESR1 (Address = 0x35). |
| 5 | ULPS_E | RW1C | 0 | ULPS Entry<br>This bit is set when either the enabled data lanes or clock lane enters ULPS. |
| 4 | ULPS_X | RW1C | 0 | ULPS Exit<br>This bit is set when all data lanes and clock lane exit from ULPS |
| 3 | FS | RW1C | 0 | Receive Frame Start Packet<br>This bit is set when CSIRX receives a frame start packet. |
| 2 | DPI | RW1C | 0 | DPI Events<br>This bit reflects the occurrence of DPI events. |
| 1 | - | RO | 0 | Reserved |
| 0 | CSI | RW1C | 0 | CSI Error Events<br>This bit is set when the CSI error event occurs. |

### 1.1.3 scape Mode and Stop State Register (ESR, Address = 0x34 ~ 0x36)

**Escape Mode and Stop State Register 0 (ESR0, Address = 0x34)**

| Bit | Name | Type | Default Value | Description |
|---|---|---|---|---|
| [7:4] | STOP | RO | HwInit | Data Lane Stopstate<br>This field reflects the input PPI signals Stopstate for the logical data lanes. |
| [3:0] | ULPS | RO | HwInit | Data Lane UlpsActiveNot<br>This field reflects the input PPI signals UlpsActiveNot for the logical data lanes.. |

**Escape Mode and Stop State Register 1 (ESR1, Address = 0x35)**

| Bit | Name | Type | Default Value | Description |
|---|---|---|---|---|
| 7 | CSTOP | RO | HwInit | Clock Lane Stopstate<br>This bit reflects the PPI signal ClkStopState. |
| 6 | CUAN | RO | HwInit | Clock Lane ULP State (Not) Active<br>The bit reflects the PPI signal ClkUlpsActiveNot. |
| 5 | RUE | RO | HwInit | Data Lane Escape Ultra-Low Power (Receive) Mode<br>This bit reflects the PPI signal RxUlpsEsc for the logical data lane#0. |
| 4 | RUCN | RO | HwInit | Clock Lane Receive Ultra-Low Power State<br>This bit reflects the PPI signal RxUlpsClkNot. |
| [3:0] | RTE | RO | HwInit | Receive Trigger Event<br>The value of this field is the bus content of the PPI signal RxTriggerEsc for the logical data lane#0. |

**Escape Mode and Stop State Register 1 (ESR1, Address = 0x36)**

| Bit | Name | Type | Default Value | Description |
|---|---|---|---|---|
| [7:4] | STOP | RO | HwInit | Data Lane Stopstate<br>This field reflects the input PPI signals Stopstate for the logical data lanes. |
| [3:0] | ULPS | RO | HwInit | Data Lane UlpsActiveNot<br>This field reflects the input PPI signals UlpsActiveNot for the logical data lanes. |

**Signal Descriptions of PPI Error Signals**

| Signal | Direction | Description |
|---|---|---|
| ErrSotHS[DLW-1:0] | Input | Start-of-Transmission (SoT) Error |
| ErrSotSyncHS[DLW-1:0] | Input | Start-of-Transmission Synchronization Error |
| ErrEotSyncHS[DLW-1:0] | Input | End-of-Transmission Synchronization Error<br>This active-high signal indicates when the last bit of a transmission doesn't match the byte boundary. |
| ErrEsc[DLW-1:0] | Input | Escape Entry Error<br>If an unrecognized escape entry command is received, this active-high signal will be asserted and remains asserted until the next change at the line state. |
| ErrControl[DLW-1:0] | Input | Receiver Data Lane Control Error<br>This active-high signal will be asserted when an incorrect line state sequence is detected at the receiver data lane. |
| ErrContentionLP0[DLW-1:0] | Input | LP0 Contention Error<br>This is PPI ErrContentionLP0 signal. |
| ErrContentionLP1[DLW-1:0] | Input | LP1 Contention Error<br>This is PPI ErrContentionLP1 signal. |